IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
DENYER ET AL.)
)
Serial No. **Not Yet Assigned**)
)
Filing Date: **Herewith**)
)
For: **IMAGE SENSORS WITH MULTIPLE**)
    INTEGRATION/READ CYCLES)
_____)

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

    Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

    Submitted herewith is a request for a proposed drawing modification as indicated in red ink to label FIG. 1(a) as prior art.

In the Claims:

    Please cancel Claims 1 to 11.

    Please add new Claims 12 to 31.

    12. A method of operating a solid state image sensing array comprising a plurality of active pixels, the method comprising:

resetting each pixel;

reading a first output from each pixel after a first period of time to obtain a first set of image data having a first dynamic range;

reading a second output from each pixel after a second period of time and without resetting each pixel to obtain a second set of image data having a second dynamic range; and

combining the first and second sets of image data to obtain a resultant set of image data having a dynamic range different from the first and second dynamic ranges.

13. A method according to Claim 12, further comprising:

reading at least a third output from each pixel after at least a third period of time and without resetting each pixel to obtain a third set of image data having a third dynamic range; and

combining at least the first, second and third sets of image data to obtain a resultant set of image data having a dynamic range different from the first, second and third dynamic ranges.

14. A method according to Claim 12, wherein the first and second periods of time are selected to be an integer multiple of a predetermined lighting flicker period.

15. A method according to Claim 12, wherein the image sensing array remains continuously exposed to incident light when the resetting is performed, and when the reading of the first and second outputs are performed.

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16. A method of operating a solid state image
sensing array comprising a plurality of active pixels, the
method comprising:

resetting and immediately reading a preliminary
output from each pixel; and

reading a first output from each pixel after a first
period of time.

17. A method according to Claim 16, further
comprising determining a difference between the preliminary
outputs and the first outputs to obtain a set of image data
substantially free of noise components represented by the
preliminary outputs.

18. A method according to Claim 16, wherein the
first period of time is selected to be an integer multiple of
a predetermined lighting flicker period.

19. A method according to Claim 16, wherein the
image sensing array remains continuously exposed to incident
light when the resetting is performed, and when the reading of
the preliminary and first outputs are performed.

20. A method according to Claim 16, further
comprising:

reading a second output from each pixel after a
second period of time and without resetting each pixel to
obtain a second set of image data having a second dynamic
range; and

determining a difference between the preliminary
outputs and each of the first, second and any subsequent

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outputs to obtain a plurality of sets of image data each of which is substantially free of noise components represented by the preliminary outputs.

21. A solid state image sensor comprising:

a plurality of active pixels;

a vertical shift register connected to rows of said plurality of active pixels;

a horizontal shift register connected to columns of said plurality of active pixels; and

scanning circuitry connected to said vertical and horizontal shift registers for reading said plurality of active pixels by resetting each pixel, reading a first output from each pixel after a first period of time to obtain a first set of image data having a first dynamic range, reading a second output from each pixel after a second period of time and without resetting each pixel to obtain a second set of image data having a second dynamic range, and combining the first and second sets of image data to obtain a resultant set of image data having a dynamic range different from the first and second dynamic ranges.

22. A solid state image sensor according to Claim 21, wherein said scanning circuitry further reads at least a third output from each pixel after at least a third period of time and without resetting each pixel to obtain a third set of image data having a third dynamic range, and combines at least the first, second and third sets of image data to obtain a resultant set of image data having a dynamic range different from the first, second and third dynamic ranges.

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23. A solid state image sensor according to Claim 21, wherein the first and second periods of time are selected to be an integer multiple of a lighting flicker period.

24. A solid state image sensor to Claim 21, wherein said image sensing array remains continuously exposed to incident light when the resetting is performed, and when the reading of the first and second outputs are performed.

25. A solid state image sensor to Claim 21, wherein said plurality of active pixels, said vertical and horizontal shift registers and said scanning circuitry are incorporated into a camera.

26. A solid state image sensor comprising:
a plurality of active pixels;
a vertical shift register connected to rows of said plurality of active pixels;
a horizontal shift register connected to columns of said plurality of active pixels; and
scanning circuitry connected to said vertical and horizontal shift registers for reading said plurality of active pixels by resetting and immediately reading a preliminary output from each pixel, and reading a first output from each pixel after a first period of time.

27. A solid state image sensor according to Claim 26, wherein said scanning circuitry determines a difference between the preliminary outputs and the first outputs to obtain a set of image data substantially free of noise components represented by the preliminary outputs.

28. A solid state image sensor according to Claim 26, wherein the first period of time is selected to be an integer multiple of a predetermined lighting flicker period.

29. A solid state image sensor according to Claim 26, wherein said image sensing array remains continuously exposed to incident light when the resetting is performed, and when the reading of the preliminary and first outputs are performed.

30. A solid state image sensor according to Claim 26, wherein said scanning circuitry further reads a second output from each pixel after a second period of time and without resetting each pixel to obtain a second set of image data having a second dynamic range, and determines a difference between the preliminary outputs and each of the first, second and any subsequent outputs to obtain a plurality of sets of image data each of which is substantially free of noise components represented by the preliminary outputs.

31. A solid state image sensor to Claim 26, wherein said plurality of active pixels, said vertical and horizontal shift registers and said scanning circuitry are incorporated into a camera.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments

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that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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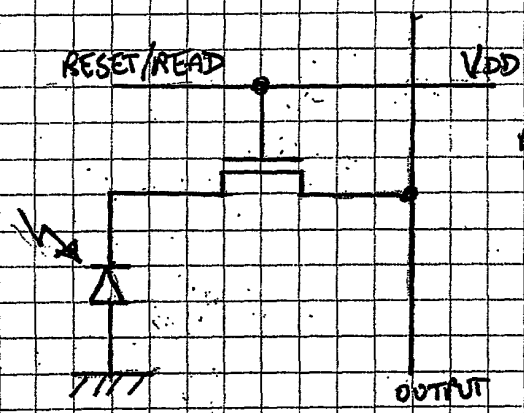407-841-2343 fax
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RESET/READ   VDD
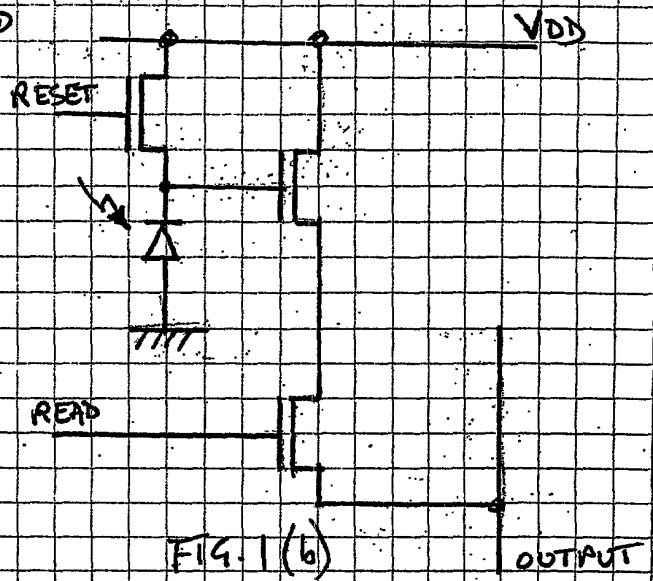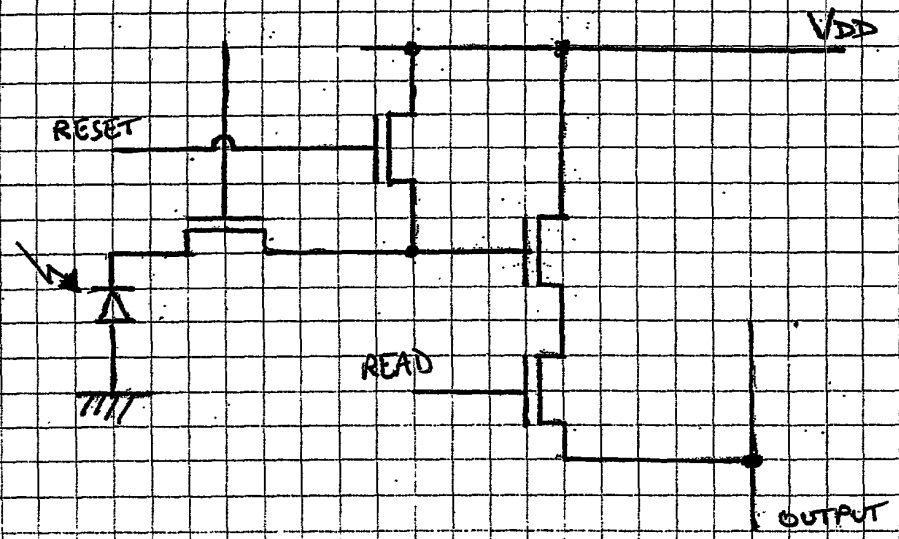
FIG. 1(a)

(PRIOR ART)

OUTPUT

RESET   VDD

READ

FIG. 1(b)   OUTPUT

RESET   VDD

READ

OUTPUT

FIG. 1(c)